In the Specification

In response to the Office Action mailed June 6, 2001, Applicants hereby correct both objections as follows: Substitute the following paragraph for the paragraph found beginning at line 20 of page 10:

FIG. 8 shows wafer portion 1300 wherein the order of the steps in method 100 has been changed such that step 120 follows step 140. That is, gate conductor 1340 has been trimmed by selective surface nitridation or oxidation (steps 122 or 124) with masking of gate conductor 1375 (step 129) after forming spacers and doping the source, drain, and gate. Accordingly, wafer portion 1300 includes gate conductor spacers 1250, which may be formed in step 120, 130, or both, and diffusion areas 1220. Wafer portion 1300 also includes a dielectric film 1360 grown on gate conductor 1340 after step 140 according to an alternative preferred embodiment of the present invention. As a further alternative, wafer portion 1300 would also be formed if gate conductor 1340 was doped, spacers 1250 formed, dielectric film 1360 grown, and then diffusion areas 1220 doped, but that option is not preferred since two doping steps are required. Dashed line 1325 indicates the dimension of the gate conductor prior to growth of dielectric film 1360 and shows that the dimension of gate conductor 1340 is reduced compared to its prior dimension. Also, FIG. 8 shows that dielectric film 1360 essentially forms a cap to isolate gate conductor 1340. In keeping with step 120, dielectric film 1360 may be removed or left in place. If left in place, then dielectric film 1360 may be useful in later forming borderless diffusion contacts as indicated in the copending patent application referenced above.